

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1 1-3 (Canceled).

1 4. (Original) An execution unit adapted to perform at least a portion of
2 the Data Encryption Standard, the execution unit comprising:

3 a) a Left Half input;

4 b) a Key input;

5 c) a Table input;

6 d) a first group of transistors configured to receive the Table input, perform
7 a table look-up, and output data;

8 e) a first exclusive-or operator having two inputs and an output, the first
9 exclusive-or operator configured to receive the Left Half input and the
10 Key input;

11 f) a second exclusive-or operator having two inputs and an output, the
12 second exclusive-or operator configured to receive the data output by the
13 first group of transistors and the output of the first exclusive-or operator;
14 and

15 g) a third exclusive-or operator having two inputs and an output, the third
16 exclusive-or operator configured to receive the Left Half input and the
17 data output by the first group of transistors.

1 5. (Original) The execution unit of claim 4, further comprising a second
2 group of transistors configured to receive data output by the second exclusive-or
3 operator.

1 6. (Original) The execution unit of claim 4, wherein the execution unit is
2 operable to perform an exclusive-or operation for a CBC mode, a CFB mode, or
3 an OFB mode of DES encryption at the same time that the first group of
4 transistors performs one or more of the following actions: receiving the table
5 input, performing the table look-up, and outputting data.

1 7. (Currently amended) An execution unit adapted to perform at least a
2 portion of the Data Encryption Standard, the execution unit comprising:

- 3 a) a Left Half input;
- 4 b) a Key input;
- 5 c) a Table input;
- 6 d) a first group of transistors configured to receive the Table input, perform
7 a table look-up, and output data;

- 8 e) a first exclusive-or operator having two inputs and an output, the first
9 exclusive-or operator configured to receive the Left Half input and the
10 Key input;
- 11 f) a second exclusive-or operator having two inputs and an output, the
12 second exclusive-or operator configured to receive the output of the first
13 group of transistors and the output of the first exclusive-or operator;
- 14 g) a third exclusive-or operator having two inputs and an output, the third
15 exclusive-or operator configured to receive the Left Half input and the
16 output of the first group of transistors and the output of the first
17 exclusive-or operator; and
- 18 h) a multiplexer, the multiplexer having two data inputs and an output, the
19 first of the two data inputs configured to receive the output of the first
20 exclusive-or operator, the second of the two data inputs configured to
21 receive the output of the second exclusive-or operator.

1 8. (Original) The execution unit of claim 7, further comprising a second
2 group of transistors configured to receive data output by the multiplexer.

1 9. (Original) The execution unit of claim 7, wherein the execution unit is
2 operable to perform an exclusive-or operation for a CBC mode, a CFB mode, or
3 an OFB mode of DES encryption at the same time that the first group of

4 transistors performs one or more of the following actions: receiving the table
5 input, performing the table look-up, and outputting data.

1 10. (Currently amended) An execution unit adapted to perform at least a
2 portion of the Data Encryption Standard, the execution unit comprising:

- 3 a) a Left Half input;
- 4 b) a Key input;
- 5 c) a Table input;
- 6 d) a Select input;
- 7 e) a first group of transistors configured to receive the Table input, perform
8 a table look-up, and output data;
- 9 f) a first exclusive-or operator having two inputs and an output, the first
10 exclusive-or operator configured to receive the Left Half input and the
11 Key input;
- 12 g) an AND operator, the AND operator having two inputs and an output, the
13 first of the two inputs of the AND operator configured to receive the
14 output of the first group of transistors, the second of the two inputs of the
15 AND operator configured to receive the Select input;
- 16 h) a second exclusive-or operator having two inputs and an output, the
17 second exclusive-or operator configured to receive the output of the AND
18 operator and the output of the first exclusive-or operator; and

19 i) a third exclusive-or operator having two inputs and an output, the third
20 exclusive-or operator configured to receive the Left Half input and the
21 output of the first group of transistors.

1 11. (Original) The execution unit of claim 10, further comprising a second
2 group of transistors configured to receive data output by the second exclusive-or
3 operator.

1 12. (Original) The execution unit of claim 10, wherein the execution unit
2 is operable to perform an exclusive-or operation for a CBC mode, a CFB mode, or
3 an OFB mode of DES encryption at the same time that the first group of
4 transistors performs one or more of the following actions: receiving the table
5 input, performing the table look-up, and outputting data.

1 13-15 (Canceled).

1 16. (Currently amended) An execution unit adapted to perform at least a
2 portion of the Data Encryption Standard, the execution unit comprising:

- 3 a) a Left Half input;
- 4 b) a Key input;
- 5 c) a Table input;

- 6 d) a Select input;
- 7 e) a first group of transistors configured to receive the Table input and the
- 8 Select input, perform a table look-up, and output, via a first output, the
- 9 result of the table look-up, the first group of transistors further configured
- 10 to output the result of the table look-up, via a second output, if the Select
- 11 input is a first value, and configured to output a zero, via the second
- 12 output, if the Select input is a second value;
- 13 f) a first exclusive-or operator having two inputs and an output, the first
- 14 exclusive-or operator configured to receive the Left Half input and the
- 15 Key input;
- 16 g) a second exclusive-or operator having two inputs and an output, the
- 17 second exclusive-or operator configured to receive the result output via
- 18 the second output of the first group of transistors and the output of the
- 19 first exclusive-or operator; and
- 20 h) a third exclusive-or operator having two inputs and an output, the third
- 21 exclusive-or operator configured to receive the result output via the first
- 22 output of the first group of transistors and the Left Half input.

1 | 17. (Currently amended) The execution unit of ~~claim 15~~ claim 16, further

2 | comprising a second group of transistors configured to receive data output by the

3 | second exclusive-or operator.

1 | 18. (Currently amended) The execution unit of ~~claim 15~~ claim 16, wherein
2 | the execution unit is operable to perform an exclusive-or operation for a CBC
3 | mode, a CFB mode, or an OFB mode of DES encryption at the same time that the
4 | first group of transistors performs one or more of the following actions: receiving
5 | the table input, performing the table look- up, and outputting data.